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TRANSMITTAL FORM *(to be used for all correspondence after initial filing)*	**Application Number**	10/613,823
	Filing Date	July 3, 2003
	In re Application of:	Mustafa EROZ et al.
	Group Art Unit	2100
	Examiner Name	Laufer
	Attorney Docket Number	10792-1139
Total Number of Pages in This Submission: 53	Client Docket Number	PD-203016

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ENCLOSURES ***(check all that apply)***

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Response
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition Routing Slip (PTO/SB/69) and Accompanying Petition
- ☐ To Convert a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Small Entity Statement
- ☐ Request of Refund
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Additional Enclosure(s) *(please identify below)*:
  - **Request for Reconsideration of Petition to Make Special Pursuant to 37 C.F.R § 1.102**

Remarks	**Should the Commissioner determine that an additional fee is due, he is hereby authorized to charge an additional fee to Deposit Account 50-0383.**

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm *or* Individual name	DITTHAVONG & CARLSON, P.C. Phouphanomketh Ditthavong, Reg. No. 44658
Signature	
Date	August 11, 2004

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Alexandria, VA 22313-1450 on this date: 8/11/04

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Signature		Date	August 11, 2004

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PATENT APPLICATION
Attorney Docket No. PD-203016
Customer No. 20991

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	
M. EROZ et al.	Group Art Unit: 2100
Application No.: 10/613,823	Examiner: Not Yet Assigned
Filed: July 3, 2003	
Title: METHOD AND SYSTEM FOR PROVIDING LOW DENSITY PARITY CHECK (LDPC) ENCODING	August 11, 2004

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attention: Special Program Examiner Laufer

REQUEST FOR RECONSIDERATION OF PETITION TO MAKE SPECIAL PURSUANT TO 37 C.F.R. § 1.102

Dear Sir:

In response to the decision on petition mailed on June 17, 2004, Applicants respectfully request reconsideration of this Petition to advance examination of this application pursuant to the provisions of 37 C.F.R. § 1.102(d) and MPEP 708.02 (VIII).

VIII. (A) Because the $130 fee has already been paid in conjunction with the original filing of this Petition on February 27, 2004, it is believed that no additional fee is due. Should the Commissioner determine that an additional fee is due, he is hereby authorized to charge the additional fee to Deposit Account 50-0383.

VIII. (B) All of the claims presented in the above-identified patent application are believed to be directed to a single invention. If the Examiner believes that the pending claims are directed to more than one invention, Applicants hereby agree to elect claims directed to a single invention, without traverse.

The present invention is directed to a method and system for encoding structured Low Density Parity Check (LDPC) codes. LDPC codes are a class of block error control codes that allow a communication system to approach the Shannon limit, which is the theoretical upper limit for data rate at a given signal to noise ratio. However, LDPC codes have not been widely deployed commercially because of their complexity and because very large blocks are required for effective use, thus causing storage problems. Therefore, it is an objective of the present invention to provide an LDPC communication system that employs simple encoding and decoding processes.

The present invention addresses this objective by providing a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code.

In another aspect of the present invention, the row indices of 1's in the column index j*360 (j=0,1,2,3, $\ldots, \frac{k_{ldpc}}{360}-1$) of the parity check matrix are given at the j^{th} row according to one of Tables 1-8:

Address of Parity Bit Accumulators (Rate 2/3)
0 10491 16043 506 12826 8065 8226 2767 240 18673 9279 10579 20928 1 17819 8313 6433 6224 5120 5824 12812 17187 9940 13447 13825 18483 2 17957 6024 8681 18628 12794 5915 14576 10970 12064 20437 4455 7151 3 19777 6183 9972 14536 8182 17749 11341 5556 4379 17434 15477 18532 4 4651 19689 1608 659 16707 14335 6143 3058 14618 17894 20684 5306 5 9778 2552 12096 12369 15198 16890 4851 3109 1700 18725 1997 15882 6 486 6111 13743 11537 5591 7433 15227 14145 1483 3887 17431 12430 7 20647 14311 11734 4180 8110 5525 12141 15761 18661 18441 10569 8192 8 3791 14759 15264 19918 10132 9062 10010 12786 10675 9682 19246 5454 9 19525 9485 7777 19999 8378 9209 3163 20232 6690 16518 716 7353 10 4588 6709 20202 10905 915 4317 11073 13576 16433 368 3508 21171 11 14072 4033 19959 12608 631 19494 14160 8249 10223 21504 12395 4322 12 13800 14161 13 2948 9647 14 14693 16027 15 20506 11082 16 1143 9020 17 13501 4014 18 1548 2190 19 12216 21556 20 2095 19897 21 4189 7958 22 15940 10048 23 515 12614 24 8501 8450 25 17595 16784 26 5913 8495 27 16394 10423 28 7409 6981 29 6678 15939 30 20344 12987 31 2510 14588 32 17918 6655 33 6703 19451 34 496 4217 35 7290 5766 36 10521 8925 37 20379 11905 38 4090 5838 39 19082 17040 40 20233 12352

41 19365 19546
42 6249 19030
43 11037 19193
44 19760 11772
45 19644 7428
46 16076 3521
47 11779 21062
48 13062 9682
49 8934 5217
50 11087 3319
51 18892 4356
52 7894 3898
53 5963 4360
54 7346 11726
55 5182 5609
56 2412 17295
57 9845 20494
58 6687 1864
59 20564 5216
0 18226 17207
1 9380 8266
2 7073 3065
3 18252 13437
4 9161 15642
5 10714 10153
6 11585 9078
7 5359 9418
8 9024 9515
9 1206 16354
10 14994 1102
11 9375 20796
12 15964 6027
13 14789 6452
14 8002 18591
15 14742 14089
16 253 3045
17 1274 19286
18 14777 2044
19 13920 9900
20 452 7374
21 18206 9921
22 6131 5414
23 10077 9726
24 12045 5479
25 4322 7990
26 15616 5550
27 15561 10661
28 20718 7387
29 2518 18804
30 8984 2600
31 6516 17909
32 11148 98
33 20559 3704
34 7510 1569

35 16000 11692
36 9147 10303
37 16650 191
38 15577 18685
39 17167 20917
40 4256 3391
41 20092 17219
42 9218 5056
43 18429 8472
44 12093 20753
45 16345 12748
46 16023 11095
47 5048 17595
48 18995 4817
49 16483 3536
50 1439 16148
51 3661 3039
52 19010 18121
53 8968 11793
54 13427 18003
55 5303 3083
56 531 16668
57 4771 6722
58 5695 7960
59 3589 14630

Table 1

Address of Parity Bit Accumulators (Rate 5/6)
0 4362 416 8909 4156 3216 3112 2560 2912 6405 8593 4969 6723
1 2479 1786 8978 3011 4339 9313 6397 2957 7288 5484 6031 10217
2 10175 9009 9889 3091 4985 7267 4092 8874 5671 2777 2189 8716
3 9052 4795 3924 3370 10058 1128 9996 10165 9360 4297 434 5138
4 2379 7834 4835 2327 9843 804 329 8353 7167 3070 1528 7311
5 3435 7871 348 3693 1876 6585 10340 7144 5870 2084 4052 2780
6 3917 3111 3476 1304 10331 5939 5199 1611 1991 699 8316 9960
7 6883 3237 1717 10752 7891 9764 4745 3888 10009 4176 4614 1567
8 10587 2195 1689 2968 5420 2580 2883 6496 111 6023 1024 4449
9 3786 8593 2074 3321 5057 1450 3840 5444 6572 3094 9892 1512
10 8548 1848 10372 4585 7313 6536 6379 1766 9462 2456 5606 9975
11 8204 10593 7935 3636 3882 394 5968 8561 2395 7289 9267 9978
12 7795 74 1633 9542 6867 7352 6417 7568 10623 725 2531 9115
13 7151 2482 4260 5003 10105 7419 9203 6691 8798 2092 8263 3755
14 3600 570 4527 200 9718 6771 1995 8902 5446 768 1103 6520
15 6304 7621
16 6498 9209
17 7293 6786
18 5950 1708
19 8521 1793
20 6174 7854
21 9773 1190
22 9517 10268

23 2181 9349
24 1949 5560
25 1556 555
26 8600 3827
27 5072 1057
28 7928 3542
29 3226 3762
0 7045 2420
1 9645 2641
2 2774 2452
3 5331 2031
4 9400 7503
5 1850 2338
6 10456 9774
7 1692 9276
8 10037 4038
9 3964 338
10 2640 5087
11 858 3473
12 5582 5683
13 9523 916
14 4107 1559
15 4506 3491
16 8191 4182
17 10192 6157
18 5668 3305
19 3449 1540
20 4766 2697
21 4069 6675
22 1117 1016
23 5619 3085
24 8483 8400
25 8255 394
26 6338 5042
27 6174 5119
28 7203 1989
29 1781 5174
0 1464 3559
1 3376 4214
2 7238 67
3 10595 8831
4 1221 6513
5 5300 4652
6 1429 9749
7 7878 5131
8 4435 10284
9 6331 5507
10 6662 4941
11 9614 10238
12 8400 8025
13 9156 5630
14 7067 8878
15 9027 3415
16 1690 3866

17 2854 8469
18 6206 630
19 363 5453
20 4125 7008
21 1612 6702
22 9069 9226
23 5767 4060
24 3743 9237
25 7018 5572
26 8892 4536
27 853 6064
28 8069 5893
29 2051 2885
0 10691 3153
1 3602 4055
2 328 1717
3 2219 9299
4 1939 7898
5 617 206
6 8544 1374
7 10676 3240
8 6672 9489
9 3170 7457
10 7868 5731
11 6121 10732
12 4843 9132
13 580 9591
14 6267 9290
15 3009 2268
16 195 2419
17 8016 1557
18 1516 9195
19 8062 9064
20 2095 8968
21 753 7326
22 6291 3833
23 2614 7844
24 2303 646
25 2075 611
26 4687 362
27 8684 9940
28 4830 2065
29 7038 1363
0 1769 7837
1 3801 1689
2 10070 2359
3 3667 9918
4 1914 6920
5 4244 5669
6 10245 7821
7 7648 3944
8 3310 5488
9 6346 9666
10 7088 6122

11 1291 7827
12 10592 8945
13 3609 7120
14 9168 9112
15 6203 8052
16 3330 2895
17 4264 10563
18 10556 6496
19 8807 7645
20 1999 4530
21 9202 6818
22 3403 1734
23 2106 9023
24 6881 3883
25 3895 2171
26 4062 6424
27 3755 9536
28 4683 2131
29 7347 8027

Table 2

Address of Parity Bit Accumulators (Rate 1/2)
54 9318 14392 27561 26909 10219 2534 8597
55 7263 4635 2530 28130 3033 23830 3651
56 24731 23583 26036 17299 5750 792 9169
57 5811 26154 18653 11551 15447 13685 16264
58 12610 11347 28768 2792 3174 29371 12997
59 16789 16018 21449 6165 21202 15850 3186
60 31016 21449 17618 6213 12166 8334 18212
61 22836 14213 11327 5896 718 11727 9308
62 2091 24941 29966 23634 9013 15587 5444
63 22207 3983 16904 28534 21415 27524 25912
64 25687 4501 22193 14665 14798 16158 5491
65 4520 17094 23397 4264 22370 16941 21526
66 10490 6182 32370 9597 30841 25954 2762
67 22120 22865 29870 15147 13668 14955 19235
68 6689 18408 18346 9918 25746 5443 20645
69 29982 12529 13858 4746 30370 10023 24828
70 1262 28032 29888 13063 24033 21951 7863
71 6594 29642 31451 14831 9509 9335 31552
72 1358 6454 16633 20354 24598 624 5265
73 19529 295 18011 3080 13364 8032 15323
74 11981 1510 7960 21462 9129 11370 25741
75 9276 29656 4543 30699 20646 21921 28050
76 15975 25634 5520 31119 13715 21949 19605
77 18688 4608 31755 30165 13103 10706 29224
78 21514 23117 12245 26035 31656 25631 30699
79 9674 24966 31285 29908 17042 24588 31857
80 21856 27777 29919 27000 14897 11409 7122
81 29773 23310 263 4877 28622 20545 22092
82 15605 5651 21864 3967 14419 22757 15896

83 30145 1759 10139 29223 26086 10556 5098
84 18815 16575 2936 24457 26738 6030 505
85 30326 22298 27562 20131 26390 6247 24791
86 928 29246 21246 12400 15311 32309 18608
87 20314 6025 26689 16302 2296 3244 19613
88 6237 11943 22851 15642 23857 15112 20947
89 26403 25168 19038 18384 8882 12719 7093
0 14567 24965
1 3908 100
2 10279 240
3 24102 764
4 12383 4173
5 13861 15918
6 21327 1046
7 5288 14579
8 28158 8069
9 16583 11098
10 16681 28363
11 13980 24725
12 32169 17989
13 10907 2767
14 21557 3818
15 26676 12422
16 7676 8754
17 14905 20232
18 15719 24646
19 31942 8589
20 19978 27197
21 27060 15071
22 6071 26649
23 10393 11176
24 9597 13370
25 7081 17677
26 1433 19513
27 26925 9014
28 19202 8900
29 18152 30647
30 20803 1737
31 11804 25221
32 31683 17783
33 29694 9345
34 12280 26611
35 6526 26122
36 26165 11241
37 7666 26962
38 16290 8480
39 11774 10120
40 30051 30426
41 1335 15424
42 6865 17742
43 31779 12489
44 32120 21001
45 14508 6996
46 979 25024

47 4554 21896	
48 7989 21777	
49 4972 20661	
50 6612 2730	
51 12742 4418	
52 29194 595	
53 19267 20113	

Table 3

Address of Parity Bit Accumulators (Rate 3/4)
0 6385 7901 14611 13389 11200 3252 5243 2504 2722 821 7374
1 11359 2698 357 13824 12772 7244 6752 15310 852 2001 11417
2 7862 7977 6321 13612 12197 14449 15137 13860 1708 6399 13444
3 1560 11804 6975 13292 3646 3812 8772 7306 5795 14327 7866
4 7626 11407 14599 9689 1628 2113 10809 9283 1230 15241 4870
5 1610 5699 15876 9446 12515 1400 6303 5411 14181 13925 7358
6 4059 8836 3405 7853 7992 15336 5970 10368 10278 9675 4651
7 4441 3963 9153 2109 12683 7459 12030 12221 629 15212 406
8 6007 8411 5771 3497 543 14202 875 9186 6235 13908 3563
9 3232 6625 4795 546 9781 2071 7312 3399 7250 4932 12652
10 8820 10088 11090 7069 6585 13134 10158 7183 488 7455 9238
11 1903 10818 119 215 7558 11046 10615 11545 14784 7961 15619
12 3655 8736 4917 15874 5129 2134 15944 14768 7150 2692 1469
13 8316 3820 505 8923 6757 806 7957 4216 15589 13244 2622
14 14463 4852 15733 3041 11193 12860 13673 8152 6551 15108 8758
15 3149 11981
16 13416 6906
17 13098 13352
18 2009 14460
19 7207 4314
20 3312 3945
21 4418 6248
22 2669 13975
23 7571 9023
24 14172 2967
25 7271 7138
26 6135 13670
27 7490 14559
28 8657 2466
29 8599 12834
30 3470 3152
31 13917 4365
32 6024 13730
33 10973 14182
34 2464 13167
35 5281 15049
36 1103 1849
37 2058 1069
38 9654 6095
39 14311 7667
40 15617 8146

41	4588	11218
42	13660	6243
43	8578	7874
44	11741	2686
0	1022	1264
1	12604	9965
2	8217	2707
3	3156	11793
4	354	1514
5	6978	14058
6	7922	16079
7	15087	12138
8	5053	6470
9	12687	14932
10	15458	1763
11	8121	1721
12	12431	549
13	4129	7091
14	1426	8415
15	9783	7604
16	6295	11329
17	1409	12061
18	8065	9087
19	2918	8438
20	1293	14115
21	3922	13851
22	3851	4000
23	5865	1768
24	2655	14957
25	5565	6332
26	4303	12631
27	11653	12236
28	16025	7632
29	4655	14128
30	9584	13123
31	13987	9597
32	15409	12110
33	8754	15490
34	7416	15325
35	2909	15549
36	2995	8257
37	9406	4791
38	11111	4854
39	2812	8521
40	8476	14717
41	7820	15360
42	1179	7939
43	2357	8678
44	7703	6216
0	3477	7067
1	3931	13845
2	7675	12899
3	1754	8187
4	7785	1400

5 9213 5891
6 2494 7703
7 2576 7902
8 4821 15682
9 10426 11935
10 1810 904
11 11332 9264
12 11312 3570
13 14916 2650
14 7679 7842
15 6089 13084
16 3938 2751
17 8509 4648
18 12204 8917
19 5749 12443
20 12613 4431
21 1344 4014
22 8488 13850
23 1730 14896
24 14942 7126
25 14983 8863
26 6578 8564
27 4947 396
28 297 12805
29 13878 6692
30 11857 11186
31 14395 11493
32 16145 12251
33 13462 7428
34 14526 13119
35 2535 11243
36 6465 12690
37 6872 9334
38 15371 14023
39 8101 10187
40 11963 4848
41 15125 6119
42 8051 14465
43 11139 5167
44 2883 14521

Table 4

Address of Parity Bit Accumulators (Rate 4/5)
0 149 11212 5575 6360 12559 8108 8505 408 10026 12828
1 5237 490 10677 4998 3869 3734 3092 3509 7703 10305
2 8742 5553 2820 7085 12116 10485 564 7795 2972 2157
3 2699 4304 8350 712 2841 3250 4731 10105 517 7516
4 12067 1351 11992 12191 11267 5161 537 6166 4246 2363
5 6828 7107 2127 3724 5743 11040 10756 4073 1011 3422
6 11259 1216 9526 1466 10816 940 3744 2815 11506 11573

7 4549 11507 1118 1274 11751 5207 7854 12803 4047 6484
8 8430 4115 9440 413 4455 2262 7915 12402 8579 7052
9 3885 9126 5665 4505 2343 253 4707 3742 4166 1556
10 1704 8936 6775 8639 8179 7954 8234 7850 8883 8713
11 11716 4344 9087 11264 2274 8832 9147 11930 6054 5455
12 7323 3970 10329 2170 8262 3854 2087 12899 9497 11700
13 4418 1467 2490 5841 817 11453 533 11217 11962 5251
14 1541 4525 7976 3457 9536 7725 3788 2982 6307 5997
15 11484 2739 4023 12107 6516 551 2572 6628 8150 9852
16 6070 1761 4627 6534 7913 3730 11866 1813 12306 8249
17 12441 5489 8748 7837 7660 2102 11341 2936 6712 11977
18 10155 4210
19 1010 10483
20 8900 10250
21 10243 12278
22 7070 4397
23 12271 3887
24 11980 6836
25 9514 4356
26 7137 10281
27 11881 2526
28 1969 11477
29 3044 10921
30 2236 8724
31 9104 6340
32 7342 8582
33 11675 10405
34 6467 12775
35 3186 12198
0 9621 11445
1 7486 5611
2 4319 4879
3 2196 344
4 7527 6650
5 10693 2440
6 6755 2706
7 5144 5998
8 11043 8033
9 4846 4435
10 4157 9228
11 12270 6562
12 11954 7592
13 7420 2592
14 8810 9636
15 689 5430
16 920 1304
17 1253 11934
18 9559 6016
19 312 7589
20 4439 4197
21 4002 9555
22 12232 7779
23 1494 8782
24 10749 3969

25 4368 3479
26 6316 5342
27 2455 3493
28 12157 7405
29 6598 11495
30 11805 4455
31 9625 2090
32 4731 2321
33 3578 2608
34 8504 1849
35 4027 1151
0 5647 4935
1 4219 1870
2 10968 8054
3 6970 5447
4 3217 5638
5 8972 669
6 5618 12472
7 1457 1280
8 8868 3883
9 8866 1224
10 8371 5972
11 266 4405
12 3706 3244
13 6039 5844
14 7200 3283
15 1502 11282
16 12318 2202
17 4523 965
18 9587 7011
19 2552 2051
20 12045 10306
21 11070 5104
22 6627 6906
23 9889 2121
24 829 9701
25 2201 1819
26 6689 12925
27 2139 8757
28 12004 5948
29 8704 3191
30 8171 10933
31 6297 7116
32 616 7146
33 5142 9761
34 10377 8138
35 7616 5811
0 7285 9863
1 7764 10867
2 12343 9019
3 4414 8331
4 3464 642
5 6960 2039
6 786 3021

7 710 2086
8 7423 5601
9 8120 4885
10 12385 11990
11 9739 10034
12 424 10162
13 1347 7597
14 1450 112
15 7965 8478
16 8945 7397
17 6590 8316
18 6838 9011
19 6174 9410
20 255 113
21 6197 5835
22 12902 3844
23 4377 3505
24 5478 8672
25 4453 2132
26 9724 1380
27 12131 11526
28 12323 9511
29 8231 1752
30 497 9022
31 9288 3080
32 2481 7515
33 2696 268
34 4023 12341
35 7108 5553

Table 5

Address of Parity Bit Accumulators (Rate 3/5)
22422 10282 11626 19997 11161 2922 3122 99 5625 17064 8270 179
25087 16218 17015 828 20041 25656 4186 11629 22599 17305 22515 6463
11049 22853 25706 14388 5500 19245 8732 2177 13555 11346 17265 3069
16581 22225 12563 19717 23577 11555 25496 6853 25403 5218 15925 21766
16529 14487 7643 10715 17442 11119 5679 14155 24213 21000 1116 15620
5340 8636 16693 1434 5635 6516 9482 20189 1066 15013 25361 14243
18506 22236 20912 8952 5421 15691 6126 21595 500 6904 13059 6802
8433 4694 5524 14216 3685 19721 25420 9937 23813 9047 25651 16826
21500 24814 6344 17382 7064 13929 4004 16552 12818 8720 5286 2206
22517 2429 19065 2921 21611 1873 7507 5661 23006 23128 20543 19777
1770 4636 20900 14931 9247 12340 11008 12966 4471 2731 16445 791
6635 14556 18865 22421 22124 12697 9803 25485 7744 18254 11313 9004
19982 23963 18912 7206 12500 4382 20067 6177 21007 1195 23547 24837
756 11158 14646 20534 3647 17728 11676 11843 12937 4402 8261 22944
9306 24009 10012 11081 3746 24325 8060 19826 842 8836 2898 5019
7575 7455 25244 4736 14400 22981 5543 8006 24203 13053 1120 5128
3482 9270 13059 15825 7453 23747 3656 24585 16542 17507 22462 14670

15627 15290 4198 22748 5842 13395 23918 16985 14929 3726 25350 24157
24896 16365 16423 13461 16615 8107 24741 3604 25904 8716 9604 20365
3729 17245 18448 9862 20831 25326 20517 24618 13282 5099 14183 8804
16455 17646 15376 18194 25528 1777 6066 21855 14372 12517 4488 17490
1400 8135 23375 20879 8476 4084 12936 25536 22309 16582 6402 24360
25119 23586 128 4761 10443 22536 8607 9752 25446 15053 1856 4040
377 21160 13474 5451 17170 5938 10256 11972 24210 17833 22047 16108
13075 9648 24546 13150 23867 7309 19798 2988 16858 4825 23950 15125
20526 3553 11525 23366 2452 17626 19265 20172 18060 24593 13255 1552
18839 21132 20119 15214 14705 7096 10174 5663 18651 19700 12524 14033
4127 2971 17499 16287 22368 21463 7943 18880 5567 8047 23363 6797
10651 24471 14325 4081 7258 4949 7044 1078 797 22910 20474 4318
21374 13231 22985 5056 3821 23718 14178 9978 19030 23594 8895 25358
6199 22056 7749 13310 3999 23697 16445 22636 5225 22437 24153 9442
7978 12177 2893 20778 3175 8645 11863 24623 10311 25767 17057 3691
20473 11294 9914 22815 2574 8439 3699 5431 24840 21908 16088 18244
8208 5755 19059 8541 24924 6454 11234 10492 16406 10831 11436 9649
16264 11275 24953 2347 12667 19190 7257 7174 24819 2938 2522 11749
3627 5969 13862 1538 23176 6353 2855 17720 2472 7428 573 15036
0 18539 18661
1 10502 3002
2 9368 10761
3 12299 7828
4 15048 13362
5 18444 24640
6 20775 19175
7 18970 10971
8 5329 19982
9 11296 18655
10 15046 20659
11 7300 22140
12 22029 14477
13 11129 742
14 13254 13813
15 19234 13273
16 6079 21122
17 22782 5828
18 19775 4247
19 1660 19413
20 4403 3649
21 13371 25851
22 22770 21784
23 10757 14131
24 16071 21617
25 6393 3725
26 597 19968
27 5743 8084
28 6770 9548
29 4285 17542
30 13568 22599
31 1786 4617
32 23238 11648
33 19627 2030
34 13601 13458

35 13740 17328
36 25012 13944
37 22513 6687
38 4934 12587
39 21197 5133
40 22705 6938
41 7534 24633
42 24400 12797
43 21911 25712
44 12039 1140
45 24306 1021
46 14012 20747
47 11265 15219
48 4670 15531
49 9417 14359
50 2415 6504
51 24964 24690
52 14443 8816
53 6926 1291
54 6209 20806
55 13915 4079
56 24410 13196
57 13505 6117
58 9869 8220
59 1570 6044
60 25780 17387
61 20671 24913
62 24558 20591
63 12402 3702
64 8314 1357
65 20071 14616
66 17014 3688
67 19837 946
68 15195 12136
69 7758 22808
70 3564 2925
71 3434 7769

Table 6

Address of Parity Bit Accumulators (Rate 8/9)
0 6235 2848 3222
1 5800 3492 5348
2 2757 927 90
3 6961 4516 4739
4 1172 3237 6264
5 1927 2425 3683
6 3714 6309 2495
7 3070 6342 7154
8 2428 613 3761
9 2906 264 5927

10 1716 1950 4273
11 4613 6179 3491
12 4865 3286 6005
13 1343 5923 3529
14 4589 4035 2132
15 1579 3920 6737
16 1644 1191 5998
17 1482 2381 4620
18 6791 6014 6596
19 2738 5918 3786
0 5156 6166
1 1504 4356
2 130 1904
3 6027 3187
4 6718 759
5 6240 2870
6 2343 1311
7 1039 5465
8 6617 2513
9 1588 5222
10 6561 535
11 4765 2054
12 5966 6892
13 1969 3869
14 3571 2420
15 4632 981
16 3215 4163
17 973 3117
18 3802 6198
19 3794 3948
0 3196 6126
1 573 1909
2 850 4034
3 5622 1601
4 6005 524
5 5251 5783
6 172 2032
7 1875 2475
8 497 1291
9 2566 3430
10 1249 740
11 2944 1948
12 6528 2899
13 2243 3616
14 867 3733
15 1374 4702
16 4698 2285
17 4760 3917
18 1859 4058
19 6141 3527
0 2148 5066
1 1306 145
2 2319 871
3 3463 1061

4 5554 6647
5 5837 339
6 5821 4932
7 6356 4756
8 3930 418
9 211 3094
10 1007 4928
11 3584 1235
12 6982 2869
13 1612 1013
14 953 4964
15 4555 4410
16 4925 4842
17 5778 600
18 6509 2417
19 1260 4903
0 3369 3031
1 3557 3224
2 3028 583
3 3258 440
4 6226 6655
5 4895 1094
6 1481 6847
7 4433 1932
8 2107 1649
9 2119 2065
10 4003 6388
11 6720 3622
12 3694 4521
13 1164 7050
14 1965 3613
15 4331 66
16 2970 1796
17 4652 3218
18 1762 4777
19 5736 1399
0 970 2572
1 2062 6599
2 4597 4870
3 1228 6913
4 4159 1037
5 2916 2362
6 395 1226
7 6911 4548
8 4618 2241
9 4120 4280
10 5825 474
11 2154 5558
12 3793 5471
13 5707 1595
14 1403 325
15 6601 5183
16 6369 4569
17 4846 896

18 7092 6184
19 6764 7127
0 6358 1951
1 3117 6960
2 2710 7062
3 1133 3604
4 3694 657
5 1355 110
6 3329 6736
7 2505 3407
8 2462 4806
9 4216 214
10 5348 5619
11 6627 6243
12 2644 5073
13 4212 5088
14 3463 3889
15 5306 478
16 4320 6121
17 3961 1125
18 5699 1195
19 6511 792
0 3934 2778
1 3238 6587
2 1111 6596
3 1457 6226
4 1446 3885
5 3907 4043
6 6839 2873
7 1733 5615
8 5202 4269
9 3024 4722
10 5445 6372
11 370 1828
12 4695 1600
13 680 2074
14 1801 6690
15 2669 1377
16 2463 1681
17 5972 5171
18 5728 4284
19 1696 1459

Table 7

Address of Parity Bit Accumulators (Rate 9/10)
0 5611 2563 2900
1 5220 3143 4813
2 2481 834 81
3 6265 4064 4265
4 1055 2914 5638

5 1734 2182 3315
6 3342 5678 2246
7 2185 552 3385
8 2615 236 5334
9 1546 1755 3846
10 4154 5561 3142
11 4382 2957 5400
12 1209 5329 3179
13 1421 3528 6063
14 1480 1072 5398
15 3843 1777 4369
16 1334 2145 4163
17 2368 5055 260
0 6118 5405
1 2994 4370
2 3405 1669
3 4640 5550
4 1354 3921
5 117 1713
6 5425 2866
7 6047 683
8 5616 2582
9 2108 1179
10 933 4921
11 5953 2261
12 1430 4699
13 5905 480
14 4289 1846
15 5374 6208
16 1775 3476
17 3216 2178
0 4165 884
1 2896 3744
2 874 2801
3 3423 5579
4 3404 3552
5 2876 5515
6 516 1719
7 765 3631
8 5059 1441
9 5629 598
10 5405 473
11 4724 5210
12 155 1832
13 1689 2229
14 449 1164
15 2308 3088
16 1122 669
17 2268 5758
0 5878 2609
1 782 3359
2 1231 4231
3 4225 2052
4 4286 3517

5 5531 3184
6 1935 4560
7 1174 131
8 3115 956
9 3129 1088
10 5238 4440
11 5722 4280
12 3540 375
13 191 2782
14 906 4432
15 3225 1111
16 6296 2583
17 1457 903
0 855 4475
1 4097 3970
2 4433 4361
3 5198 541
4 1146 4426
5 3202 2902
6 2724 525
7 1083 4124
8 2326 6003
9 5605 5990
10 4376 1579
11 4407 984
12 1332 6163
13 5359 3975
14 1907 1854
15 3601 5748
16 6056 3266
17 3322 4085
0 1768 3244
1 2149 144
2 1589 4291
3 5154 1252
4 1855 5939
5 4820 2706
6 1475 3360
7 4266 693
8 4156 2018
9 2103 752
10 3710 3853
11 5123 931
12 6146 3323
13 1939 5002
14 5140 1437
15 1263 293
16 5949 4665
17 4548 6380
0 3171 4690
1 5204 2114
2 6384 5565
3 5722 1757
4 2805 6264

5	1202	2616
6	1018	3244
7	4018	5289
8	2257	3067
9	2483	3073
10	1196	5329
11	649	3918
12	3791	4581
13	5028	3803
14	3119	3506
15	4779	431
16	3888	5510
17	4387	4084
0	5836	1692
1	5126	1078
2	5721	6165
3	3540	2499
4	2225	6348
5	1044	1484
6	6323	4042
7	1313	5603
8	1303	3496
9	3516	3639
10	5161	2293
11	4682	3845
12	3045	643
13	2818	2616
14	3267	649
15	6236	593
16	646	2948
17	4213	1442
0	5779	1596
1	2403	1237
2	2217	1514
3	5609	716
4	5155	3858
5	1517	1312
6	2554	3158
7	5280	2643
8	4990	1353
9	5648	1170
10	1152	4366
11	3561	5368
12	3581	1411
13	5647	4661
14	1542	5401
15	5078	2687
16	316	1755
17	3392	1991

Table 8

In another aspect of the present invention, the row indices of 1's in other column indices m (m modulo 360 $\neq 0$ and m < k_{ldpc}) of the parity check matrix are given by $\{x + m \bmod 360 \times q\} \bmod (n_{ldpc} - k_{ldpc})$, where q=60 for rate 2/3 LDPC code, q=30 for rate 5/6 LDPC code, q=90 for rate 1/2 LDPC code, q=45 for rate 3/4 LDPC code, q=36 for rate 4/5 LDPC code, q=72 for rate 3/5 LDPC code, q=20 for rate 8/9 LDPC code, q=18 for rate 9/10 LDPC code, wherein x denotes an entry at the j^{th} row of Tables 1-7, where j=int{m/360}, and int{.} denotes the integer function, the row indices of 1's in the column index m=$k_{ldpc}+j$ (j=0,1,2,…,n_{ldpc}-k_{ldpc}-2) of the parity check matrix being given by j and j+1, the row index of 1 in the column index n_{ldpc}-1 of the parity check matrix being given by n_{ldpc}-k_{ldpc}-1.

VIII. (C) A pre-examination search was conducted by a professional search firm. The search was conducted in Class 375, subclasses 259, 261, 265, 268, 269, 272, and 279; Class 714, subclasses 752, 758, 781, and 782; and on computer using Delphion, EPO ESPACE, and PTO databases; and on the Internet. In addition, an International Search Report (ISR) for corresponding International Patent Application No. PCT/US03/21073 has been issued by the European Patent Office (EPO) acting as the International Search Authority.

VIII. (D) The pre-examination search revealed the following references:

(i) U.S. Patent No. 6,567,465

(ii) U.S. Patent Application Publication No. US 2003/0203721 A1

(iii) U.S. Patent Application Publication No. US 2003/0187899 A1

(iv) U.S. Patent Application Publication No. US 2003/0014718 A1

(v) International Publication No. WO 03/088504 A1

(vi) International Publication No. WO 03/065591 A2

The International Search Report cited the following additional references:

(vii) European Patent Application No. EP 1 093 231 A1

(viii) International Publication No. WO 02/099976 A2

(ix) S. Johnson et al., "Construction of Low-Density Parity-Check Codes from Kirkman Triple Systems", Proceedings, IEEE Global Telecommunications Conference 2001, pp. 970-974, November 25-29, 2001

(x) T. Richardson et al., "Efficient Encoding of Low-Density Parity Check Codes", IEEE Transactions on Information Theory, Vol. 47, No. 2, pp. 638-656, February 2001

(xi) L. Ping et al., "Low Density Parity Check Codes with Semi-Random Parity Check Matrix", Electronics Letters, IEEE Stevenage, Vol. 35, No. 1, pp. 38-39, January 7, 1999

(xii) B. Vasic et al, "Kirkman Systems and Their Application in Perpendicular Magnetic Recording", IEEE Transactions on Magnetics, Vol. 38, No. 4, pp. 1705-1710, July 2002

(xiii) R. Echard et al., "The Pi-Rotation Low-Density Parity Check Codes", Proceedings, IEEE Global Telecommunications Conference 2001, pp. 980-984, November 25-29, 2001

(xiv) B. Vasic, "Combinatorial Constructions of Low-Density Parity Check Codes for Iterative Decoding", Proceedings, IEEE International Symposium on Information Theory 2002, p. 312, June 30-July 5, 2002

(xv) B. Vasic, "Structured Iteratively Decodable Codes Based on Steiner Systems and Their Application in Magnetic Recording", Proceedings, IEEE Global Telecommunications Conference 2001, pp. 2954-2960, November 25-29, 2001

Each of these references is included in the Information Disclosure Statement, along with a copy of each reference. A copy of the International Search Report is included with this Petition for the convenience of the Examiner.

VIII. (E) A discussion of the above-listed references is provided below:

(i) United States Patent No. 6,567,465 relates to a DSL modem with a received and a transmitter that includes an LDPC encoder which utilizes a generation matrix G which is derived from a substantially deterministic H matrix in order to generate redundant parity bit for a block of bits. The inventors recognize that the prior art approaches (i.e., Gallager's random distribution, and IBM Corporation's deterministic procedure) to designing H matrices have undesirable characteristics with respect to their implementation in DSL standards. In particular, the random distribution approach of Gallager is not reproducible (as it is random), and thus, the H matrix used by the transmitting modem must be conveyed to the receiving modem. Because the H matrix is typically a very large matrix, the transfer of this information is undesirable. On the other hand, while the deterministic matrix of IBM is reproducible, it is extremely complex and difficult to generate. Thus, considerable processing power must be dedicated to generating such a matrix, thereby adding complexity and cost to the DSL modem.

The DSL modem of the inventors' generally includes a receiver and a transmitter with the transmitter including a substantially deterministic LDPC encoder. The encoder is a function of a substantially deterministic H matrix (H=A|B). More particularly, the encoder takes a block of bits and utilizes a generation matrix $G=A^{-1}B$ which is derived from (i.e., is a function of) the H matrix in order to generate redundant parity bits. The redundant bits are appended to the original block of bits to generate a word.

A substantially deterministic H matrix may be determined according to the steps of FIG. 3. First, at step 102 the "ones" of a first column N_j are assigned randomly or deterministically. Preferably, the "ones" are distributed evenly within the first column with the first "1" in the first row of the first column according to the following relationship: $H(r,1)=1$, where $r=1+(i-1)*\text{integer}(M_j/N_j)$; $i=1,2,\ldots N_j$, where M_j is the number of rows in the matrix and N_j is the number of "ones" in the column. Thus, if the "ones" are assigned deterministically, the first "one" is located at H(1,1) and the remainder of "ones" for the column are evenly distributed in the column. If, on the other hand, the "ones" are assigned randomly, preferably, a "one" is located in a random row of column 1, and the remaining "ones" are evenly distributed. While less preferred, all "ones" in column one can be randomly located.

When generating descendants it is possible that one or more descendants can "disappear" because of the lack of free positions satisfying the rectangle elimination criterium. This determination can be made at step 115 (shown in phantom after step 108). To regenerate the "lost descendant", it is generally sufficient to change the order of descendant generation for that column (step 117--shown in phantom). Thus, if the order of descendant generation was conducted "bottom-up", the direction of generation

is switched to "top-down" and vice versa. Preferably, the order of descendant generation is changed only for that column. If changing the order of descendant generation in a column does not cause a free position to appear, the descendant disappears for that column.

However, United States Patent No. 6,567,465 fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code. Additionally, United States Patent No. 6,567,465 fails to disclose the row indices of 1's in the column index j*360 (j=0,1,2,3, $\ldots, \frac{k_{ldpc}}{360}-1$) of the parity check matrix are given at the j^{th} row according to one of Tables 1-8. Further, there is no disclosure that the row indices of 1's in other column indices m (m modulo 360 $\neq$ 0 and m < k_{ldpc}) of the parity check matrix are given by $\{x + m \bmod 360 \times q\} \bmod (n_{ldpc} - k_{ldpc})$, where q=60 for rate 2/3 LDPC code, q=30 for rate 5/6 LDPC code, q=90 for rate 1/2 LDPC code, q=45 for rate 3/4 LDPC code, q=36 for rate 4/5 LDPC code, q=72 for rate 3/5 LDPC code, q=20 for rate 8/9 LDPC code, q=18 for rate 9/10 LDPC code, wherein x denotes an entry at the j^{th} row of Tables 1-7, where

j=int{m/360}, and int{.} denotes the integer function, the row indices of 1's in the column index m=$k_{ldpc}+j$ (j=0,1,2,...,n_{ldpc}-k_{ldpc}-2) of the parity check matrix being given by j and j+1, the row index of 1 in the column index n_{ldpc}-1 of the parity check matrix being given by n_{ldpc}-k_{ldpc}-1.

(ii) United States Patent Application Publication No. US 2003/0203721 A1 relates to a method for generating an adaptive air interface waveform that comprises generating a waveform that include a variable carrier frequency and variable bandwidth signal. The authors recognize that current wireless communication systems do not adjust well to dynamic changes in the electromagnetic spectrum. The authors describe a heteromorphic waveform that dynamically adapts in frequency, time, modulation, code, data rate, power, signaling, and multi-carrier organization. The waveform will increase spectral efficiency by enabling efficient, opportunistic and cooperative spectrum use. It reacts to time-varying channel and use conditions by seizing time/frequency/spatial "holes" and using the most efficient coding, modulation, signaling and multi-carrier organization consistent with non-interfering communications. The heteromorphic waveform of the invention is subdivided into two major components as follows. Adaptive Multi-Carrier Organization and Signaling configures a variable carrier frequency and variable bandwidth signal into one or many sub-carriers that are dynamically placed over a span of up to 250 MHz to avoid or minimize interference with transmissions of existing spectrum users. Each sub-carrier is independently modulated by direct sequence spread-spectrum (DS SS) for variable spreading and coding gain against cooperative, non-cooperative, and threat signals. A combination time/code pilot is

embedded within the waveform to empower optimization based on sub-carrier channel estimates. The waveform supports a broad range of adaptive/hybrid multiple access schemes including combinations of CDMA, TDMA, FDMA, and FHMA. Adaptive Multi-Level Bandwidth-Efficient Coding and Modulation (BECM) provides a family of BECM schemes, incorporating both multi-constellation modulation and forward error-correction coding. A Low Density Parity-Check Code (LDPC) coded modulation family will be used to advance the state-of-the-art in bandwidth efficiency and adaptation capability. Adapting the modulation constellation, code rate, and code length to match the available spectrum and sub-carrier conditions will maximize spectral efficiency while meeting quality of service (QoS) and data rate needs.

However, United States Patent Application Publication No. US 2003/0203721 A1 fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code. Additionally, United States Patent Application Publication No. US 2003/0203721 A1 fails to disclose the row indices of 1's in the column index j*360 (j=0,1,2,3, $\ldots, \frac{k_{ldpc}}{360}-1$) of the parity

check matrix are given at the j^{th} row according to one of Tables 1-8. Further, there is no disclosure that the row indices of 1's in other column indices m (m modulo 360 $\neq 0$ and m < k_{ldpc}) of the parity check matrix are given by $\{x + m \bmod 360 \times q\} \bmod (n_{ldpc} - k_{ldpc})$, where q=60 for rate 2/3 LDPC code, q=30 for rate 5/6 LDPC code, q=90 for rate 1/2 LDPC code, q=45 for rate 3/4 LDPC code, q=36 for rate 4/5 LDPC code, q=72 for rate 3/5 LDPC code, q=20 for rate 8/9 LDPC code, q=18 for rate 9/10 LDPC code, wherein x denotes an entry at the j^{th} row of Tables 1-7, where j=int{m/360}, and int{.} denotes the integer function, the row indices of 1's in the column index m=k_{ldpc}+j (j=0,1,2,...,n_{ldpc}-k_{ldpc}-2) of the parity check matrix being given by j and j+1, the row index of 1 in the column index n_{ldpc}-1 of the parity check matrix being given by n_{ldpc}-k_{ldpc}-1.

(iii) United States Patent Application Publication No. US 2003/0187899 A1 relates to a matrix operation processing device. In the matrix operation P=HxI^T, obtaining a process result P using N bits of a signal data string I and NxM bits of a check matrix H, process delay and circuit scale are reduced by performing necessary operations for each column of the check matrix H and accumulating the result for each row. In particular, in a check matrix for error correcting codes needed for coding, the number of the columns M of the check matrix is far smaller than the number of the rows N. Therefore, by calculating a plurality of pieces of data in each column in parallel and accumulating the result for each row, the number of adders and circuit scale can be reduced. The matrix operation processing device comprises a storage unit storing a process result P, such as a register or the like; a storage unit storing a check matrix H, such as a ROM or the like; a unit reading the check matrix H and process result P when

an address counter or the like receives a signal data string I and controlling the storage; and an operation unit, such as an adder or the like. The device obtains column data, the input data which must be processed every time the device receives a signal data string I, from H, reads necessary items of a target process result P, multiplies the received data by the necessary items and writes the result back into the storage unit as the process result P. By repeating this process for all the full received data of the signal data string I, a process result P can be obtained.

However, United States Patent Application Publication No. US 2003/0187899 A1 fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code. Additionally, United States Patent Application Publication No. US 2003/0187899 A1 fails to disclose the row indices of 1's in the column index j*360 (j=0,1,2,3, $\ldots,\frac{k_{ldpc}}{360}-1$) of the parity check matrix are given at the j^{th} row according to one of Tables 1-8. Further, there is no disclosure that the row indices of 1's in other column indices m (m modulo 360 $\neq 0$ and m < k_{ldpc}) of the parity check matrix are given by $\{x + m \bmod 360 \times q\} \bmod (n_{ldpc} - k_{ldpc})$,

where q=60 for rate 2/3 LDPC code, q=30 for rate 5/6 LDPC code, q=90 for rate 1/2 LDPC code, q=45 for rate 3/4 LDPC code, q=36 for rate 4/5 LDPC code, q=72 for rate 3/5 LDPC code, q=20 for rate 8/9 LDPC code, q=18 for rate 9/10 LDPC code, wherein x denotes an entry at the j^{th} row of Tables 1-7, where j=int{m/360}, and int{.} denotes the integer function, the row indices of 1's in the column index m=$k_{ldpc}+j$ (j=0,1,2,...,n_{ldpc}-k_{ldpc}-2) of the parity check matrix being given by j and j+1, the row index of 1 in the column index n_{ldpc}-1 of the parity check matrix being given by n_{ldpc}-k_{ldpc}-1.

(iv) United States Patent Application Publication No. US 2003/0014718 A1 relates to a computer-implemented system and method for generating LDPC codes. The authors are concerned with the following design problem. Given positive integers {a}=(a_1, a_2, . . . , a_n), {b}=(b_1, b_2, . . . , b_m), n, and m; construct a mxn parity check matrix H with the largest possible girth such that H has exactly a_j ones in each column j=1,2, . . . , n, at most b_r ones in row r=1, 2, . . . , m. The authors utilize a heuristic "Bit-Filling" algorithm for the above problem. Accordingly, a method is proposed for generating high rate LDPC codes that first constructs a matrix H of size mxn having m rows of check nodes and n columns of bit nodes. The matrix meets the following requirements: the weight of the j^{th} column equals a_j; each row, r has weight at most b_r; and the matrix H can be represented by a Tanner graph that has girth of at least g greater than or equal to g. The method then iteratively adds an $(n+1)^{th}$ column U_1 to matrix H, wherein the size of U_1 is initially empty and is at most a_{n+1}, and wherein U_1 comprises a set of i check nodes such that i is greater than or equal to zero and i is less than a_{n+1}. The method then iteratively adds check nodes to U_1 such that each check node does not violated

predetermined girth and check-degree constraints. The matrix H is updated when a new column is added. The iterations are terminated if there are no new check nodes that do not violate the girth and check-degree constraints. The method can be modified to optimize various parameters, including the following cases: maximizing the rate for a fixed girth; maximizing the girth for a fixed rate; and maximizing the rate for a fixed girth and a fixed length.

However, United States Patent Application Publication No. US 2003/0014718 A1 fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code. Additionally, United States Patent Application Publication No. US 2003/0014718 A1 fails to disclose the row indices of 1's in the column index j*360 (j=0,1,2,3, $\ldots, \frac{k_{ldpc}}{360}-1$) of the parity check matrix are given at the j^{th} row according to one of Tables 1-8. Further, there is no disclosure that the row indices of 1's in other column indices m (m modulo 360 $\neq$ 0 and m < k_{ldpc}) of the parity check matrix are given by $\{x + m \bmod 360 \times q\} \bmod (n_{ldpc} - k_{ldpc})$, where q=60 for rate 2/3 LDPC code, q=30 for rate 5/6 LDPC code, q=90 for rate 1/2

LDPC code, q=45 for rate 3/4 LDPC code, q=36 for rate 4/5 LDPC code, q=72 for rate 3/5 LDPC code, q=20 for rate 8/9 LDPC code, q=18 for rate 9/10 LDPC code, wherein x denotes an entry at the j^{th} row of Tables 1-7, where j=int{m/360}, and int{.} denotes the integer function, the row indices of 1's in the column index m=$k_{ldpc}+j$ (j=0,1,2,...,n_{ldpc}-k_{ldpc}-2) of the parity check matrix being given by j and j+1, the row index of 1 in the column index n_{ldpc}-1 of the parity check matrix being given by n_{ldpc}-k_{ldpc}-1.

(v) International Publication No. WO 03/088504 A1 relates to a method for decoding error correcting codes, wherein a decoded data block is associated with coded data according to a global code comprising at least two sub-codes. An irregular bipartite graph is associated with the global code, the decoding method is iterative, and a data block to be decoded is distributed between a plurality of disjointed memory banks which can be independently addressed. The method also comprises, at each iteration, a stage for feeding in parallel at least two decoders which respectively correspond to at least one of the sub-codes, in terms of the data to be decoded, the data to be decoded being extracted in parallel from at least two of the memory banks in order to feed the same amount of decoders, and each decoder is sequentially fed with the data to be decoded corresponding thereto. The publication also relates to a corresponding coding method, corresponding coding/decoding devices, and a corresponding signal.

However, International Publication No. WO 03/088504 A1 fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences

of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code. Additionally, International Publication No. WO 03/088504 A1 fails to disclose the row indices of 1's in the column index j*360 (j=0,1,2,3, $\ldots, \frac{k_{ldpc}}{360}-1$) of the parity check matrix are given at the j^{th} row according to one of Tables 1-8. Further, there is no disclosure that the row indices of 1's in other column indices m (m modulo 360 $\neq 0$ and m < k_{ldpc}) of the parity check matrix are given by $\{x + m \bmod 360 \times q\} \bmod (n_{ldpc} - k_{ldpc})$, where q=60 for rate 2/3 LDPC code, q=30 for rate 5/6 LDPC code, q=90 for rate 1/2 LDPC code, q=45 for rate 3/4 LDPC code, q=36 for rate 4/5 LDPC code, q=72 for rate 3/5 LDPC code, q=20 for rate 8/9 LDPC code, q=18 for rate 9/10 LDPC code, wherein x denotes an entry at the j^{th} row of Tables 1-7, where j=int{m/360}, and int{.} denotes the integer function, the row indices of 1's in the column index m=$k_{ldpc}+j$ (j=0,1,2,...,n_{ldpc}-k_{ldpc}-2) of the parity check matrix being given by j and j+1, the row index of 1 in the column index n_{ldpc}-1 of the parity check matrix being given by n_{ldpc}-k_{ldpc}-1.

(vi) International Publication No. WO 03/065591 A2 relates to a method and apparatus for decoding digital information transmitted through the communication channel or recorded on a recording medium. The method and apparatus are preferably

applied in the systems where data is encoded using regular LDPC codes with parity check matrices composed from circulants (a matrix is called a circulant if all of its columns or rows are cyclic shifts of each other). A class of codes is constructed from integer lattices. In combinatorics a design is a pair (*V*, *B*), where *V* is a set of some elements called points, and B is a collection of subsets of *V* called blocks. The number of points and blocks are denoted later by $v=|V|$ and $b=|B|$, respectively. If $T \leq v$ is an integer parameter, such that any subset of *T* points from *V* is contained in exactly λ blocks, a *T*-design is dealt with. A Balanced Incomplete Block Design (BIBD) is a *T*-design such that each block contains the same number of points *k*, and every point is contained in the same number of blocks *r*. The authors use a novel construction of the BIBD based on 2-dimensional integer lattices.

However, International Publication No. WO 03/065591 A2 fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code. Additionally, International Publication No. WO 03/065591 A2 fails to disclose the row indices of 1's in the column index *j**360

(j=0,1,2,3, ..., $\frac{k_{ldpc}}{360}-1$) of the parity check matrix are given at the j^{th} row according to one of Tables 1-8. Further, there is no disclosure that the row indices of 1's in other column indices m (m modulo 360 $\neq 0$ and m < k_{ldpc}) of the parity check matrix are given by $\{x + m \bmod 360 \times q\} \bmod (n_{ldpc} - k_{ldpc})$, where q=60 for rate 2/3 LDPC code, q=30 for rate 5/6 LDPC code, q=90 for rate 1/2 LDPC code, q=45 for rate 3/4 LDPC code, q=36 for rate 4/5 LDPC code, q=72 for rate 3/5 LDPC code, q=20 for rate 8/9 LDPC code, q=18 for rate 9/10 LDPC code, wherein x denotes an entry at the j^{th} row of Tables 1-7, where j=int{m/360}, and int{.} denotes the integer function, the row indices of 1's in the column index m=k_{ldpc}+j (j=0,1,2,...,n_{ldpc}-k_{ldpc}-2) of the parity check matrix being given by j and j+1, the row index of 1 in the column index n_{ldpc}-1 of the parity check matrix being given by n_{ldpc}-k_{ldpc}-1.

(vii) European Patent Application No. 1 093 231 A1 relates to a construction method for LDPC codes, and simple systematic coding of LDPC codes. The LDPC coding procedure codes M information symbols with N-M redundant (i.e., parity check) symbols which has the same minimum number of nonzero elements in each row and less than two rows or columns with only one nonzero value.

However, European Patent Application No. EP 1 093 231 A1 fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the

rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code. Additionally, European Patent Application No. EP 1 093 231 A1 fails to disclose the row indices of 1's in the column index j*360 (j=0,1,2,3, $\ldots, \frac{k_{ldpc}}{360}-1$) of the parity check matrix are given at the j^{th} row according to one of Tables 1-8. Further, there is no disclosure that the row indices of 1's in other column indices m (m modulo 360 $\neq$ 0 and m < k_{ldpc}) of the parity check matrix are given by $\{x + m \bmod 360 \times q\} \bmod (n_{ldpc} - k_{ldpc})$, where q=60 for rate 2/3 LDPC code, q=30 for rate 5/6 LDPC code, q=90 for rate 1/2 LDPC code, q=45 for rate 3/4 LDPC code, q=36 for rate 4/5 LDPC code, q=72 for rate 3/5 LDPC code, q=20 for rate 8/9 LDPC code, q=18 for rate 9/10 LDPC code, wherein x denotes an entry at the j^{th} row of Tables 1-7, where j=int{m/360}, and int{.} denotes the integer function, the row indices of 1's in the column index m=k_{ldpc}+j (j=0,1,2,…,n_{ldpc}-k_{ldpc}-2) of the parity check matrix being given by j and j+1, the row index of 1 in the column index n_{ldpc}-1 of the parity check matrix being given by n_{ldpc}-k_{ldpc}-1.

(viii) International Publication No. WO 02/099976 A2 relates to a method of generating low density parity check codes for encoding data that includes constructing a parity check matrix H from a balanced incomplete block design in which a plurality of B-sets which define the matrix have no more than one intersection point. The parity bits are

then generated as a function of the constructed parity check matrix H. A combinatorial construction of a class of high rate iteratively decodable codes using Balanced Incomplete Block Design (BIBD), in particular Steiner (v, 3, 1)-systems, is proposed. This construction gives parity check matrices with column weights of 3 and minimum girths of 4, 6 and higher. These systems are constructed using cyclic difference families of z_v with $v \equiv 1 \bmod 6$, v prime power.

However, International Publication No. WO 02/099976 A2 fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code. Additionally, International Publication No. WO 02/099976 A2 fails to disclose the row indices of 1's in the column index *j**360 (*j*=0,1,2,3, $\ldots, \frac{k_{ldpc}}{360}-1$) of the parity check matrix are given at the j^{th} row according to one of Tables 1-8. Further, there is no disclosure that the row indices of 1's in other column indices m (m modulo 360 $\neq$ 0 and m < k_{ldpc}) of the parity check matrix are given by $\{x + m \bmod 360 \times q\} \bmod (n_{ldpc} - k_{ldpc})$, where *q*=60 for rate 2/3 LDPC code, *q*=30 for rate 5/6 LDPC code, *q*=90 for rate 1/2 LDPC code, *q*=45 for rate 3/4 LDPC code, *q*=36 for

rate 4/5 LDPC code, q=72 for rate 3/5 LDPC code, q=20 for rate 8/9 LDPC code, q=18 for rate 9/10 LDPC code, wherein x denotes an entry at the j^{th} row of Tables 1-7, where j=int{m/360}, and int{.} denotes the integer function, the row indices of 1's in the column index m=$k_{ldpc}+j$ (j=0,1,2,...,n_{ldpc}-k_{ldpc}-2) of the parity check matrix being given by j and j+1, the row index of 1 in the column index n_{ldpc}-1 of the parity check matrix being given by n_{ldpc}-k_{ldpc}-1.

(ix) The article entitled "Construction of Low-Density Parity-Check Codes from Kirkman Triple Systems" by Johnson et al. relates to a construction method for regular LDPC codes based on combinatorial designs known as Kirkman triple systems. The authors have observed that analytically constructed LDPC codes comprise only a very small subset of possible codes, and as result, most LDPC codes are constructed randomly. A key idea in the paper is that the absence of cycles of length 4 in the Tanner graph associated with an LDPC code can be systematically avoided by taking as parity-check matrices the incidence matrices of suitably chosen combinatorial designs. For small block lengths in particular, an analytic construction method that guarantees (1) small, uniform row and column weights, and (2) the absence of 4-cycles, is expected to be particularly useful. The authors use a class of designs called Kirkman triple systems (KTS) to derive regular (v, b, ρ, 3, {1,0})-designs. Kirkman triple systems are defined as the resolvable Steiner triple systems. That is, the blocks of a Kirkman triple system can be arranged into ρ groups such that the v/3 blocks of each group are disjoint, and each group contains every point precisely once. Consequently, if all blocks in a group are removed from H what remains is a parity-check matrix H_0 with v parity checks, row

weight ρ-1 and n = $b - v/3$. The above construction method produces parity-check matrices having constant column and row weight and girth of at least 6. These (3, ρ)-regular codes can be constructed for any number of parity-check sums $m \equiv 3(\mathrm{mod}\,6)$, and for all row weights $\rho \in \{1, 2, \ldots, (m\text{-}1)/2\}$.

However, the article entitled "Construction of Low-Density Parity-Check Codes from Kirkman Triple Systems" fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code. Additionally, the article fails to disclose the row indices of 1's in the column index j*360 (j=0,1,2,3, $\ldots, \frac{k_{ldpc}}{360} - 1$) of the parity check matrix are given at the j^{th} row according to one of Tables 1-8. Further, there is no disclosure that the row indices of 1's in other column indices m (m modulo 360 $\neq 0$ and m < k_{ldpc}) of the parity check matrix are given by $\{x + m \bmod 360 \times q\} \bmod (n_{ldpc} - k_{ldpc})$, where q=60 for rate 2/3 LDPC code, q=30 for rate 5/6 LDPC code, q=90 for rate 1/2 LDPC code, q=45 for rate 3/4 LDPC code, q=36 for rate 4/5 LDPC code, q=72 for rate 3/5 LDPC code, q=20 for rate 8/9 LDPC code, q=18 for rate 9/10 LDPC code, wherein x denotes an entry at the j^{th} row of Tables 1-7, where

j=int{m/360}, and int{.} denotes the integer function, the row indices of 1's in the column index m=k_{ldpc}+j (j=0,1,2,...,n_{ldpc}-k_{ldpc}-2) of the parity check matrix being given by j and j+1, the row index of 1 in the column index n_{ldpc}-1 of the parity check matrix being given by n_{ldpc}-k_{ldpc}-1.

(x) The article entitled "Efficient Encoding of Low-Density Parity-Check Codes" by T. Richardson et al. relates to the encoding problem for LDPC codes, and more generally to the encoding problem for codes specified by sparse parity-check matrices. An approach for exploiting the sparseness of the parity-check matrix to obtain efficient encoders is presented. The authors aim to show that, even without cascade constructions or restrictions on the shape of the parity-check matrix, the encoding complexity is quite manageable in most cases and provably linear in many cases. For the (3,6)-regular LDPC code, for example, the complexity of encoding is essentially quadratic in the block length. However, it is shown that the associated coefficient can be made quite small, so that encoding codes even of length n ≈ 100,000 is still quite practical. It is also shown that "optimized" codes actually admit linear time encoding.

The proposed encoding procedure entails two steps: a preprocessing step and the actual encoding step. In the preprocessing step, the authors first perform row and column permutations to bring the parity-check matrix into approximate lower triangular form with as small a gap g as possible. A check is performed to determine whether $\phi = -ET^{-1}B + D$ is nonsingular. The authors note that there is little hope of finding the optimal row and column permutations which result in the minimum gap, given that they are interested in large block lengths. Thus, the authors utilize greedy algorithms.

However, the article entitled "Efficient Encoding of Low-Density Parity-Check Codes" fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code. Additionally, the article fails to disclose the row indices of 1's in the column index j*360 (j=0,1,2,3, $\ldots,\frac{k_{ldpc}}{360}-1$) of the parity check matrix are given at the j^{th} row according to one of Tables 1-8. Further, there is no disclosure that the row indices of 1's in other column indices m (m modulo 360 $\neq 0$ and m < k_{ldpc}) of the parity check matrix are given by $\{x+m \bmod 360\times q\}\bmod(n_{ldpc}-k_{ldpc})$, where q=60 for rate 2/3 LDPC code, q=30 for rate 5/6 LDPC code, q=90 for rate 1/2 LDPC code, q=45 for rate 3/4 LDPC code, q=36 for rate 4/5 LDPC code, q=72 for rate 3/5 LDPC code, q=20 for rate 8/9 LDPC code, q=18 for rate 9/10 LDPC code, wherein x denotes an entry at the j^{th} row of Tables 1-7, where j=int{m/360}, and int{.} denotes the integer function, the row indices of 1's in the column index m=k_{ldpc}+j (j=0,1,2,...,n_{ldpc}-k_{ldpc}-2) of the parity check matrix being given by j and j+1, the row index of 1 in the column index n_{ldpc}-1 of the parity check matrix being given by n_{ldpc}-k_{ldpc}-1.

(xi) The article entitled "Low Density Parity Check Codes with Semi-Random Parity Check Matrix" by L. Ping et al. relates to a semi-random approach to LDPC code design. The semi-random technique, i.e., only part of H is generated randomly, and the remaining part is deterministic. With binary codes, codeword **c** as **c**= |**p**, **d**|^T where **p** and **d** contain the parity and information bits, respectively. Accordingly, H is decomposed into $\mathbf{H} = [\mathbf{H}^p, \mathbf{H}^d]$. $\mathbf{H}^p$ is constructed in some deterministic form (and must be a square matrix). $\mathbf{H}^d$ has sub-blocks $\mathbf{H}^{d_i}$, $i = 1, 2, \ldots t$, wherein one element 1 per column and $kt/(n-k)$ 1s per row are randomly created.

However, the article entitled "Low Density Parity Check Codes with Semi-Random Parity Check Matrix" fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code. Additionally, the article fails to disclose the row indices of 1's in the column index j*360 (j=0,1,2,3, $\ldots,\frac{k_{ldpc}}{360}-1$) of the parity check matrix are given at the j^{th} row according to one of Tables 1-8. Further, there is no disclosure that the row indices of 1's in other

column indices m (m modulo 360 $\neq 0$ and m < k_{ldpc}) of the parity check matrix are given by $\{x + m \bmod 360 \times q\} \bmod (n_{ldpc} - k_{ldpc})$, where q=60 for rate 2/3 LDPC code, q=30 for rate 5/6 LDPC code, q=90 for rate 1/2 LDPC code, q=45 for rate 3/4 LDPC code, q=36 for rate 4/5 LDPC code, q=72 for rate 3/5 LDPC code, q=20 for rate 8/9 LDPC code, q=18 for rate 9/10 LDPC code, wherein x denotes an entry at the j^{th} row of Tables 1-7, where j=int{m/360}, and int{.} denotes the integer function, the row indices of 1's in the column index m=k_{ldpc}+j (j=0,1,2,…,n_{ldpc}-k_{ldpc}-2) of the parity check matrix being given by j and j+1, the row index of 1 in the column index n_{ldpc}-1 of the parity check matrix being given by n_{ldpc}-k_{ldpc}-1.

(xii) The article entitled "Kirkman Systems and Their Application in Perpendicular Magnetic Recording" by B. Vasic et al. relates to an introduction of a novel class of very high-rate LDPC codes. A systematic way of constructing codes is based on Kirkman systems. Given a (v, k, λ)-CDF with t base blocks $B_i = \{b_{i,1} \ldots\ldots b_{i,k}\}, 1 \le i \le t$, the authors construct a parity check matrix H=[H_1 H_2 … H_t] from the circulant submatrices H_i, 1≤ i ≤ t, which have the size v x v, and full rank v. The equation $\sum_{i=1}^{t-1} H_i \cdot \overline{c_i}^{Tr} = H_t \cdot \overline{p}^{Tr}$ leads to a simple hardware implementation of the encoding process. The encoder processes independently all data words computing products $\beta_i = H_i \cdot \overline{c_i}^{Tr}$, and then calculates the left hand-side of $\sum_{i=1}^{t-1} H_i \cdot \overline{c_i}^{Tr} = H_t \cdot \overline{p}^{Tr}$, $\beta_1 + \beta_2 + \ldots + \beta_{t-1} = \beta$. Since all matrices H_i, 1≤ i ≤ t-1, are circulant, the calculation of each vector β_i requires a shift register of length v, and v logic units consisting of an AND gate, EXCLUSIVE OR gate, and a flip-flop. The

inverse of the matrix H_t is precalculated and stored in ROM. In fact, since the inverse of a circulant matrix is also circulant, the memory required for storing H_t^{-1} is not v^2, but only v (only one column of H_t^{-1} needs to be stored).

However, the article entitled "Kirkman Systems and Their Application in Perpendicular Magnetic Recording" fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code. Additionally, the article fails to disclose the row indices of 1's in the column index j*360 (j=0,1,2,3, $\ldots, \frac{k_{ldpc}}{360}-1$) of the parity check matrix are given at the j^{th} row according to one of Tables 1-8. Further, there is no disclosure that the row indices of 1's in other column indices m (m modulo 360 $\neq 0$ and m < k_{ldpc}) of the parity check matrix are given by $\{x + m \bmod 360 \times q\} \bmod (n_{ldpc} - k_{ldpc})$, where q=60 for rate 2/3 LDPC code, q=30 for rate 5/6 LDPC code, q=90 for rate 1/2 LDPC code, q=45 for rate 3/4 LDPC code, q=36 for rate 4/5 LDPC code, q=72 for rate 3/5 LDPC code, q=20 for rate 8/9 LDPC code, q=18 for rate 9/10 LDPC code, wherein x denotes an entry at the j^{th} row

of Tables 1-7, where j=int{m/360}, and int{.} denotes the integer function, the row indices of 1's in the column index m=$k_{ldpc}+j$ (j=0,1,2,...,$n_{ldpc}-k_{ldpc}-2$) of the parity check matrix being given by j and $j+1$, the row index of 1 in the column index $n_{ldpc}-1$ of the parity check matrix being given by $n_{ldpc}-k_{ldpc}-1$.

(xiii) The article entitled "The Pi-Rotation Low-Density Parity Check Codes" by R. Echard et al. relates to an introduction of an ensemble of quasi-regular LDPC error control codes called π-rotation LDPC codes. The authors create a parity check matrix composed of two sub-matrices, $\mathbf{H} = [\mathbf{H}^p|\mathbf{H}^d]$. $\mathbf{H}^p$ is an n-k by n-k square matrix and $\mathbf{H}^d$ is an n-k by k matrix. $\mathbf{H}^p$ is a dual-diagonal pattern. The construction of $\mathbf{H}^d$ is presented as a composition of a q by t array of m by m random permutation matrices. A random permutation matrix is simply the identity matrix with randomly permuted columns. The dimension of $\mathbf{H}^d$ is qm by tm inducing a code length of $(q+t)m$, an information length of tm and a code rate of $t/(q+t)$. $\mathbf{H}^d$ is created based on a single permutation vector, which defines the π-rotation pattern. An efficient coding scheme and circuit design based on the single permutation are presented. Simulation results indicate that these codes perform as well as regular LDPC codes based on completely random matrix constructions. These features make the pi-rotation code valuable for practical communication system implementation.

However, the article entitled "The Pi-Rotation Low-Density Parity Check Codes" fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents

occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code. Additionally, the article fails to disclose the row indices of 1's in the column index j*360 (j=0,1,2,3, $\ldots,\frac{k_{ldpc}}{360}-1$) of the parity check matrix are given at the j^{th} row according to one of Tables 1-8. Further, there is no disclosure that the row indices of 1's in other column indices m (m modulo 360 $\neq 0$ and m < k_{ldpc}) of the parity check matrix are given by $\{x+m \bmod 360 \times q\} \bmod (n_{ldpc}-k_{ldpc})$, where q=60 for rate 2/3 LDPC code, q=30 for rate 5/6 LDPC code, q=90 for rate 1/2 LDPC code, q=45 for rate 3/4 LDPC code, q=36 for rate 4/5 LDPC code, q=72 for rate 3/5 LDPC code, q=20 for rate 8/9 LDPC code, q=18 for rate 9/10 LDPC code, wherein x denotes an entry at the j^{th} row of Tables 1-7, where j=int{m/360}, and int{.} denotes the integer function, the row indices of 1's in the column index m=$k_{ldpc}+j$ (j=0,1,2,...,n_{ldpc}-k_{ldpc}-2) of the parity check matrix being given by j and j+1, the row index of 1 in the column index n_{ldpc}-1 of the parity check matrix being given by n_{ldpc}-k_{ldpc}-1.

(xiv) The article entitled "Combinatorial Constructions of Low-Density Parity Check Codes for Iterative Decoding" by B. Vasic relates to a method for a combinatorial construction of regular LDPC codes based on balanced incomplete block designs, or

more specifically on cyclic difference families of Abelian groups and affine geometries. Several constructions are presented, and the bounds on minimal distance are derived by using the concept of Pasch configurations. In particular, the author presents two constructions for "deterministic" LDPC codes. The first one is based on difference families and the Z_v group, while the second construction is based on a rectangular lattice finite geometry. The first method exploits Netto and Buratti difference families, and gives a BIBD with $v \equiv 1 \bmod 6$, v power of a prime. With respect to the second construction, the number of parity bits is equal to *mk*, *m*-a prime, and the blocks are defined as lines of different slopes connecting points of a *m*x*k* integer lattice.

However, the article entitled "Combinatorial Constructions of Low-Density Parity Check Codes for Iterative Decoding" fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code. Additionally, the Vasic article fails to disclose the row indices of 1's in the column index j*360 (j=0,1,2,3, $\ldots, \frac{k_{ldpc}}{360}-1$) of the parity check matrix are given at the j^{th} row according to one of Tables 1-8. Further, there is no disclosure that the row

indices of 1's in other column indices m (m modulo 360 $\neq 0$ and m < k_{ldpc}) of the parity check matrix are given by $\{x + m \bmod 360 \times q\} \bmod (n_{ldpc} - k_{ldpc})$, where q=60 for rate 2/3 LDPC code, q=30 for rate 5/6 LDPC code, q=90 for rate 1/2 LDPC code, q=45 for rate 3/4 LDPC code, q=36 for rate 4/5 LDPC code, q=72 for rate 3/5 LDPC code, q=20 for rate 8/9 LDPC code, q=18 for rate 9/10 LDPC code, wherein x denotes an entry at the j^{th} row of Tables 1-7, where j=int{m/360}, and int{.} denotes the integer function, the row indices of 1's in the column index m=k_{ldpc}+j (j=0,1,2,...,n_{ldpc}-k_{ldpc}-2) of the parity check matrix being given by j and j+1, the row index of 1 in the column index n_{ldpc}-1 of the parity check matrix being given by n_{ldpc}-k_{ldpc}-1.

(xv) The article entitled "Structured Iteratively Decodable Codes Based on Steiner Systems and Their Application in Magnetic Recording" relates to a method for a combinatorial construction of a class of iteratively decodable codes The author proposes codes that are based on Steiner triple systems and the Z_v group, where v is the number of parity check equations describing the code. Balanced incomplete block design using Netto's difference families with $v \equiv 1 \bmod 6$, v prime power. The encoding algorithm exploits the cyclic structure of the balanced incomplete block design. Let V be an additive Abelian group of order v. Then t k-element subsets of G, $B_i = \{b_{i,1}, \ldots, b_{i,k}\}$ $1 \leq i \leq t$ form a (v, k, λ) difference family (DF) if every nonzero element of G can be represented exactly λ ways as a difference of two elements lying in a same member of a family, i.e., occurs λ times among the differences $b_{i,m} - b_{j,n}$, $1 \leq i, j \leq k$, $1 \leq m, n \leq k$.

The sets B_1 are called based blocks. If V is isomorphic with Z_v, a group of integers modulo v, then a (v, k, λ) DF is called a cyclic difference family (CDF).

However, the article entitled "Structured Iteratively Decodable Codes Based on Steiner Systems and Their Application in Magnetic Recording" fails to disclose a combination of method and structure for generating LDPC codes that comprises storing information representing a structured parity check matrix of the LDPC codes, the information being organized in tabular form, wherein each row represents occurrences of one values within a first column of a group of columns of the parity check matrix, the rows correspond to groups of columns of the parity check matrix, wherein subsequent columns within each of the groups are derived according to a predetermined operation; and preferably also encoding an input signal using BCH codes, wherein the output LDPC coded signal corresponding to the input signal represents a code having an outer BCH code and an inner BCH code. Additionally, the article fails to disclose the row indices of 1's in the column index j*360 (j=0,1,2,3, $\ldots, \frac{k_{ldpc}}{360}-1$) of the parity check matrix are given at the j^{th} row according to one of Tables 1-8. Further, there is no disclosure that the row indices of 1's in other column indices m (m modulo 360 $\neq 0$ and m < k_{ldpc}) of the parity check matrix are given by $\{x + m \bmod 360 \times q\} \bmod (n_{ldpc} - k_{ldpc})$, where q=60 for rate 2/3 LDPC code, q=30 for rate 5/6 LDPC code, q=90 for rate 1/2 LDPC code, q=45 for rate 3/4 LDPC code, q=36 for rate 4/5 LDPC code, q=72 for rate 3/5 LDPC code, q=20 for rate 8/9 LDPC code, q=18 for rate 9/10 LDPC code, wherein x denotes an entry at the j^{th} row of Tables 1-7, where j=int{m/360}, and int{.} denotes the integer function, the row indices of 1's in the column index m=k_{ldpc}+j (j=0,1,2,…,n_{ldpc}-

k_{ldpc}-2) of the parity check matrix being given by j and j+1, the row index of 1 in the column index n_{ldpc}-1 of the parity check matrix being given by n_{ldpc}-k_{ldpc}-1.

CONCLUSION

It is respectfully requested that examination of the above-referenced application be advanced in accordance with the provisions of 37 C.F.R. § 1.102 and MPEP 708.02.

Applicants' undersigned attorney may be reached by telephone at (301) 601-7252. All correspondence should continue to be directed to our address given below.

Respectfully submitted,

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August 11, 2004

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